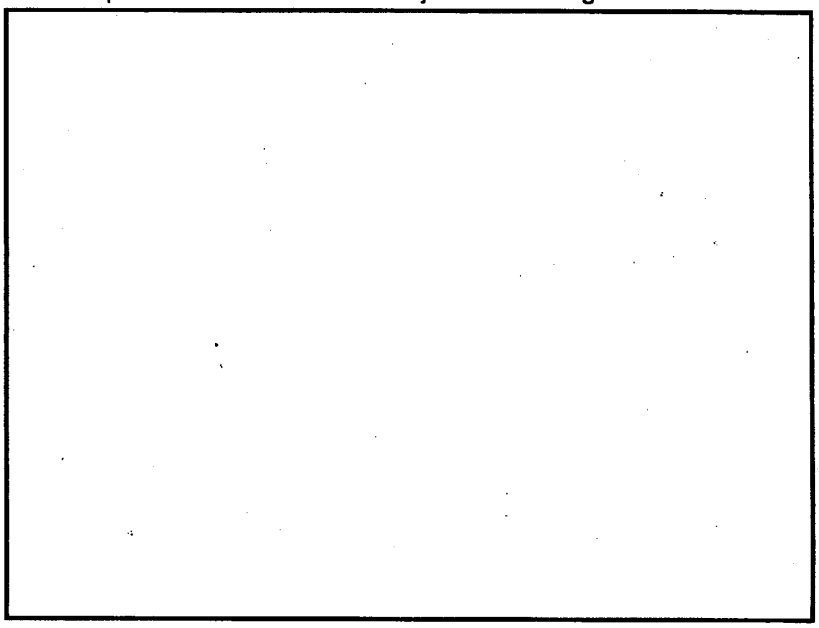
Pre.	S. Uchida	Rev	L	K. Kuroda
Apr.	M.Tabata 26-Oct.-'01			M.Tabata 24-Jul.-'03

Notice : This is not a final specification. Some parametric limits are subject to change.

CM1400DU-24NF



- Ic 1400A
- V_{CES} 1200V
- Insulated Type
- 2-elements in a pack

APPLICATION

UPS & General purpose inverters

E

ABSOLUTE MAXIMUM RATINGS (T_j = 25 °C)

Symbol	Item	Conditions	Ratings	Units	
V_{CES}	Collector-emitter voltage	G-E Short	1200	V	
V_{GES}	Gate-emitter voltage	C-E Short	±20	V	
I_C	Collector current	DC, Tc'= 94 °C *1	1400	A	I
I_{CM}		Pulse ②	2800		
I_E ①	Emitter current		1400	A	I
I_{EM} ①		Pulse ②	2800		
Pc ③	Maximum collector dissipation	Tc = 25 °C	3900	W	E G
Tj	Junction temperature		−40~+150	°C	
Tstg	Storage temperature*4		−40~+125	°C	K
Viso	Isolation voltage	Main terminal to base plate,AC 1 min.	2500	V	
—	Torque strength	Main terminal M6	3.5 ~ 4.5	N·m	
—	Torque strength	Mounting holes M6	3.5 ~ 4.5	N·m	
—	Weight	Typical value	1400	g	

ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Units	
I_{CES}	Collector cutoff current	$V_{CE}=V_{CES}, V_{GE}$= 0V	–	–	1	mA	E
$V_{GE(th)}$	Gate-emitter threshold voltage	I_C=140mA, V_{CE}= 10V	6	7	8	V	E
I_{GES}	Gate leakage current	$V_{GE}=V_{GES}$, V_{CE}= 0V	–	–	1.5	μA	J
$V_{CE(sat)}$ (chip)	Collector to emitter saturation voltage (without lead resistance)	T_j= 25 °C, I_C = 1400A	–	1.8	2.5	V	G
		T_j= 125 °C, V_{GE}= 15V ④	–	2.0	–		
R(lead)	Module lead resistance	I_C = 1400A, terminal-chip	–	0.286	–	mΩ	L
Cies	Input capacitance	V_{CE}= 10V, V_{GE}= 0V	–	–	220	nF	E
Coes	Output capacitance		–	–	25		E
Cres	Reverse transfer capacitance		–	–	4.7		E
Q_G	Total gate charge	V_{CC}=600V, Ic=1400A, V_{GE}=15V	–	7200	–	nC	
td(on)	Turn-on delay time	V_{CC}=600V, Ic=1400A	–	–	800	ns	E H
tr	Turn-on rise time	$V_{GE1}=V_{GE2}$=15V	–	–	300		E
td(off)	Turn-off delay time	R_G=0.22Ω, Inductive load	–	–	1000		E
tf	Turn-off fall time	switching operation	–	–	300		E
Trr ①	Reverse recovery time	I_E=1400A	–	–	700	ns	E H
Qrr ①	Reverse recovery charge		–	90	–	μC	E H
V_{EC} ① (chip)	Emitter-collector voltage (without lead resistance)	I_E=1400A, V_{GE}= 0V	–	–	3.2	V	E J K
Rth(j-c)Q	Thermal resistance*3	IGBT part (1/2module)	–	–	0.032	°C/W	G
Rth(j-c)R		FWDi part (1/2module)	–	–	0.053		
Rth(j-c')Q	Thermal resistance*1	Tc measured point is just under the chips(IGBT part)	–	–	0.014	°C/W	
Rth(j-c')R		Tc measured point is just under the chips(FWDi part)	–	–	0.023		
Rth(c-f)	Contact thermal resistance*2	Case to fin, Thermal compound Applied (1/2module)	–	0.016	–		
RG	External gate resistance		0.22	–	2.2	Ω	F H

*1: Tc' measured point is just under the chips.
If you use this value , Rth(f-a) should be measured just under the chips.
*2: Typical value is measured by using Shin-etsu Silicone "G-746".
*3: Tc measured point is shown in page "3-3".
*4: The operation temperature is restrained by the permission temperature of female connector. K

① I_E, V_{EC}, trr & Qrr represent characteristics of the anti-parallel, emitter to collector free-wheel diode (FWDi).

② Pulse width and repetition rate should be such that the device junction temp.(Tj) dose not exceed Tjmax rating.

③ Junction temperature (T_j) should not increase beyond 150°C.

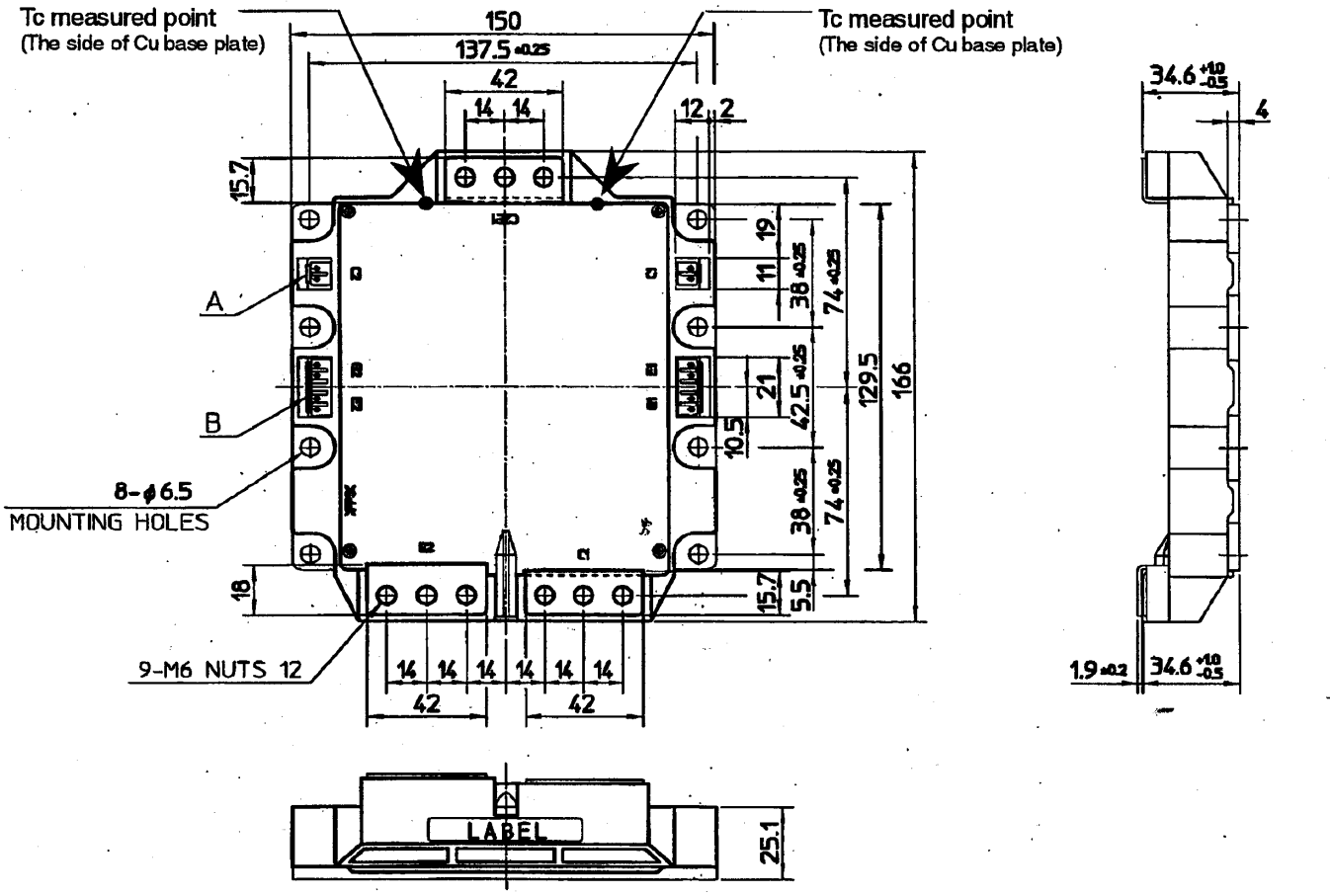
④ Pulse width and repetition rate should be such as to cause neglible temperature rise.

OUTLINE DRAWING

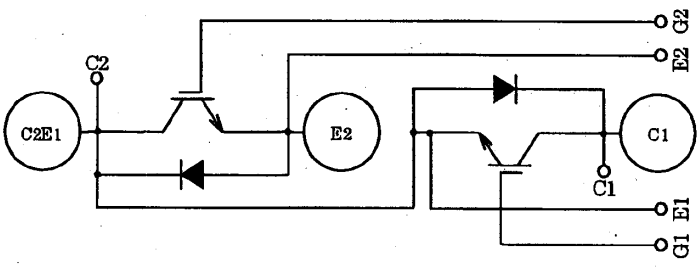
Dimensions in mm

B
C
F
G

A,B HOUSING Type
(J.S.T.Mfg.Co,Ltd)
A : VHR-2N
B : VHR-5N



CIRCUIT DIAGRAM



Terminal name

G